In the Abstract:

Insert a new abstract as follows:

A separate link instruction register is connected in series in a test data and instruction data scan path on an IC. Instruction data shifted into the register provides control signals and selective enable signals for testing one selected core wrapper of plural core wrappers on the IC. Test data passes around the link instruction register. The control signals include a clock signal, a shift signal, a capture signal, and an update signal. The control signals also include an enable signal for each core wrapper. Additional link instruction registers may be arranged in a hierarchy for testing cores embedded within other cores.